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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/682,166	10/10/2003	Koichi Ishimi	67161-116	8198

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EXAMINER	
NGUYEN, LINH M	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 02/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)	
Office Action Summary	10/682,166	ISHIMI, KOICHI	
	Examiner	**Art Unit**	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3,4,6-9,11-17,19-26,55-62 and 75-79* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6,8,9,11,12,15-17,19-26,55-62 and 75-79* is/are allowed.

6)☒ Claim(s) *3,4,7,13 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/27/06*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

This is a reply to the Applicant's amendment submitted on 01/27/2006. By virtue of this amendment, claims 3-4, 6-9, 11-17, 19-26, 55-62 and 75-79 are now pending.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 3-4, and 13-14 are rejected under 35 U.S.C. 103(a) 35 U.S.C. 103(a) as being unpatentable over Yen (U.S. Patent No. 6,501,307) in view of Applicant Admitted Prior Art *(See Remarks, filed 09/07/2005, pgs. 20-21)*.

With respect to claim 3, Yen discloses, in Figs. 2 and 7B, a clock generation circuit comprising a frequency-multiplying circuit [14] receiving an input of a reference clock signal and outputting a same or frequency-multiplied clock signal of the reference clock signal, a buffering portion [20] buffering the clock signal, the buffering portion includes at least one buffer circuit buffering the clock signal such that a logic low period and a logic high period of the clock signal are different from each other [Fig. 7B].

Yen fails to disclose that at least one of a power supply potential or a ground potential in the buffer circuit is different from another power supply voltage or ground voltage in the buffering portion.

The Applicant admitted that the technology of using a control signal to vary the power supply potential and the ground potential of a buffer circuit is well-known, such technology is implemented in devices such as "Longrun2" of Transmeta Corporation and "Extended Intel SpeedStep" in Pentium M of Intel Corporation *(see Remarks filed 09/07/2005, page 21)*.

To configure the circuit of Yen with a buffer circuit having a control signal to vary a power or ground potential of a buffer circuit would have been obvious to one of ordinary in the art at the time of the invention since such configuration would provide potential control versatility as taught by the Applicant Admitted Prior Art.

With respect to claim 4, Yen discloses, in Fig. 2, a clock generation circuit comprising a frequency-multiplying circuit [14] receiving an input of a reference clock signal and outputting a same or frequency-multiplied clock signal of the reference clock signal.

Yen fails to disclose a buffering portion buffering the clock signal, the buffering portion includes at least one buffer circuit buffering the clock signal such that a logic low period and a logic high period of the clock signal are different from each other, and a substrate potential of a transistor included in the buffer circuit is different from a substrate potential of another transistor included in the buffering portion.

The Applicant admitted that the technology of controlling the threshold voltage Vth by varying the substrate voltage of transistors in a buffer circuit is well-known, this technology has been used in the VT-CMOS technology and others; controlling the threshold voltage Vth by varying the substrate voltage is described by T. Kuroda, et al. *(see Remarks filed 09/07/2005, page 21)*.

To configure the circuit of Yen with a buffer circuit having different substrate potential between transistors would have been obvious to one of ordinary in the art at the time of the invention since such configuration would provide variable threshold voltage control as taught by the Applicant Admitted Prior Art.

With respect to claim 13, Yen discloses, in Figs. 2 and 7B, a clock generation circuit comprising a frequency-multiplying circuit [14] receiving an input of a reference clock signal and outputting a same or frequency-multiplied clock signal of the reference clock signal; and a buffering portion [20] buffering the clock signal, in which the buffering portion includes at least one buffer circuit for changing a duty ratio [shown in Fig. 7B] of the clock signal.

Yen fails to show at least one of a power supply potential and a ground potential of the buffer circuit varies using a control signal.

The Applicant admitted that the technology of using a control signal to vary the power supply potential and the ground potential of a buffer circuit is well-known, such technology is implemented in such devices as "Longrun2" of Transmeta Corporation and "Extended Intel SpeedStep" in Pentium M of Intel Corporation *(see Remarks filed 09/07/2005, page 21).*

To configure the circuit of Yen with a buffer circuit having a control signal to vary a power or ground potential of a buffer circuit would have been obvious to one of ordinary in the art at the time of the invention since such configuration would provide potential control versatility as taught by the Applicant Admitted Prior Art.

With respect to claim 14, Yen discloses, in Figs. 2 and 7B, a clock generation circuit comprising a frequency-multiplying circuit [14] receiving an input of a reference clock signal and outputting a same or frequency-multiplied clock signal of the reference clock signal; and a buffering portion [20] buffering the clock signal and the buffering portion includes at least one buffer circuit for changing a duty ratio of the output clock signal.

Yen fails to disclose a substrate potential of a transistor included in buffer circuit varies using a control signal.

The Applicant admitted that the technology of using a control signal to vary the substrate potential of a transistor included in a buffer circuit is well-known, this technology has been used in the VT-CMOS technology and others; controlling the threshold voltage Vth by varying the substrate voltage is described by T. Kuroda, et al. *(see Remarks filed 09/07/2005, page 21).*

To configure the circuit of Yen with a buffer circuit having a control signal to vary a substrate potential of a transistor would have been obvious to one of ordinary in the art at the time of the invention since such configuration would provide versatility in variable threshold voltage control as taught by the Applicant Admitted Prior Art.

3. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yen (U.S. Patent No. 6,501,307) in view of Suda (U.S. Pub. No. 2004/0247066.

With respect to claim 7, Yen discloses, in Fig. 2, a clock generation circuit comprising a frequency-multiplying circuit [14] receiving an input of a reference clock signal and outputting a same or frequency-multiplied clock signal of the reference clock signal, the clock signal having a logic high period and a logic low period different from each other [Fig. 7B]; and a buffering portion [20] buffering the clock signal.

Yen fails to teach the frequency-multiplied circuit includes a) a ring oscillator, b) a comparator comparing a phase of the clock signal output from the ring oscillator with a phase of the reference clock signal, c) a counter determining a digital count value based on a phase comparison result output from the comparator, and the ring oscillator including first and second delay lines connected in series for receiving the digital count value for determining a delay time, and a selector selecting and outputting an input from one of the first and second delay lines in accordance with said clock signal.

Suda discloses, in Figs. 1 and 16, paragraph [0264], lines 6-8, a frequency multiplier including a) a ring oscillator [3], b) a comparator [1] comparing a phase of the clock signal output from the ring oscillator with a phase of the reference clock signal, c) a counter [2] determining a digital count value based on a phase comparison result output from the comparator, and the ring oscillator including first and second delay lines *(from 115)* connected in series for receiving the digital count value for determining a delay time, and a selector [116] selecting and outputting an input from one of the first and second delay lines in accordance with said clock signal.

To configure the circuit of Yen with a frequency multiplier as taught by Suda which have small power consumption would have been obvious to one of ordinary skill in the art at the time of the invention since Suda teaches that such configuration of the frequency multiplier can be readily reduced in size, enable a locked loop in a high band and have high reliability *(see Suda, paragraph [0023], lines 3-5).*

Allowable Subject Matter

4. Claims 6, 8-9, 11-12, 15-17, 19-26, 55-62 and 75-79 are allowed.

5. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art of record does not show or fairly suggest:

a) A clock generation circuit including a control circuit incrementing/decrementing a digital count value in response to a rising/falling of a reference clock signal, and a ring oscillator including a delay line varying a delay time in accordance with the digital count value, in combination with the remaining claimed limitations, as called for in claims 6, 19 and 79;

b) A clock generation circuit, in which in a duty ratio control signal, a period of time during which both of clock signal and the duty ratio control signal are logic high is different from the other period of time, in combination with the remaining claimed limitations, as called for in claim 8;

c) A clock generation circuit, in which in a duty ratio control signal, a period of time during which both of clock signal and the duty ratio control signal are logic low is different from the other period of time, in combination with the remaining claimed limitations, as called for in claim 9;

d) A clock generation circuit, in which a plurality of first transistors connected in parallel between a power supply node and an output node and having one polarity and a driving capability control portion controlling on/off of the plurality of first and second transistors respectively using a plurality of driving capability control signals, in combination with the remaining claimed limitations, as called for in claim 11;

e) A clock generation circuit, in which a timing control portion controlling rising or falling timing of a signal level output from a first inverter circuit to a second inverter circuit using a plurality of timing control signals, in combination with the remaining claimed limitations, as called for in claim 12;

f) A clock generation circuit, in which a delay circuit capable of controlling a delay time using a delay control signal and a logic element receiving an output signal from the delay circuit and the reference clock signal for outputting a clock signal, in combination with the remaining claimed limitations, as called for in claim 15;

g) A clock generation circuit, in which a logic element receiving a selector control signal and a clock signal for outputting a select signal, in combination with the remaining claimed limitations, as called for in claim 22;

h) A clock generation circuit, in which in a duty ratio control signal, a period of time during which both of clock signal and the duty ratio control signal are logic high and the other period of time varies, in combination with the remaining claimed limitations, as called for in claim 25;

i) A clock generation circuit, in which in a duty ratio control signal, a period of time during which both of clock signal and the duty ratio control signal are logic low and the other period of time varies, in combination with the remaining claimed limitations, as called for in claim 26;

j) A system including a current measurement circuit measuring an operating current of a circuit receiving clock signal, in which a central processing unit controls a duty ratio of the clock signal or on/off of duty ratio control based on a measurement result of the operating current, in combination with the remaining claimed limitations, as called for in claims 55 and 56;

k) A system including a temperature measurement circuit measuring a temperature of a circuit receiving clock signal, in which a central processing unit controls a duty ratio of the clock signal or on/off of duty ratio control based on a measurement result of the temperature, in combination with the remaining claimed limitations, as called for in claims 59 and 60; and

l) A system, in which a duty ratio of a clock signal can be set by an instruction from a central processing unit, individually for the clock signal being supplied to a module circuit and for the clock signal being supplied to a prescribed external circuit, in combination with the remaining claimed limitations, as called for in claims 75 and 76.

Remarks

6. Applicant's argument filed 01/27/2006 has been seriously considered but not completely persuasive.

Regarding Applicant's arguments with respect to claims 3, 4, 13 and 14, on page 25, second paragraph, the Applicant state that "*the Examiner did not provide any support for respective claims 3, 4, 13 and 14 that AAPA teaches the limitations recited in those claims*". The examiner disagrees. The support has been shown by the statement, at end of page 4 bridging page 5 in the office action dated 10/25/2005, "The Applicant admitted that the technology of using a control signal to vary the power supply potential and the ground potential of a buffer circuit is well-known, such technology is implemented in devices such as "Longrun2" of Transmeta Corporation and "Extended Intel SpeedStep" in Pentium M of Intel Corporation *(see Remarks filed 09/07/2005, page 21")".*

Regarding Applicant's arguments still with respect to claims 3, 4, 13 and 14, on page 25, second paragraph and again on page 26, third paragraph, the Applicant challenges the examiner to show motivation to modify Yen's circuit based on AAPA to arrive at the claimed invention. First, motivation has been provided in the office action; and second, it is not necessary that the cited references or prior art actually suggest expressly or in so many words, the changes or improvements that the Applicant has made. The test for combining references is what the references as a whole would have suggested to one of ordinary skill in the art. In re Sheckier, 168 USPQ 716 (CCPA 1971) : In re McLaughlin 170 I USPQ 209 (CCPA 1971); In re Young 159 USPQ 725 (CCPA 1968).

Regarding Applicant's arguments with respect to claims 6, 19-21 and 79, on page 27, last paragraph, the examiner finds that the argument is persuasive; hence, claims 6, 19-21 and 79 are now allowed.

With respect to Applicant's argument regarding claim 7, at page 29, first paragraph, in response to Applicant's argument base on a theoretical scenario "*if selector 116 were removed from the delay line of Suda, the delay line would become no longer a delay line*", the examiner disagrees, this is incorrect since if the selector 116 were removed from the delay line of Suda, the delay line would still be a delay line but with maximum delay and without variation in the range of delay.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN

LINH MY NGUYEN
PRIMARY EXAMINER